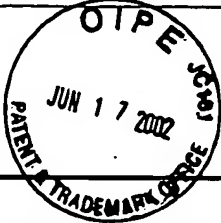


Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)			Attorney Docket No.: 4640.P006		Application Number: 10/083,241	
Page 1 of 2			First Named Inventor: Yervant Zorian		RECEIVED JUN 24 2002 Technology Center 2100	
			Filing Date: February 25, 2002			
U.S. PATENT DOCUMENTS						
Exam. Initial ^a	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Patent of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
DT		5,513,318		van de Goor et al.	4-30-1996	
DT		5,570,374		Yau et al.	10-29-1996	
DT		5,960,009		Gizopoulos et al.	9-28-1999	
DT		5,978,935		Kim et al.	11-2-1999	
DT		5,978,947		Kim et al.	11-2-1999	
DT		6,085,334		Giles et al.	7-4-2000	
DT		6,205,564	B1	Kim et al.	3-20-2001	
DT		6,237,123	B1	Kim et al.	5-22-2001	
DT		6,317,846	B1	Higgins et al.	11-13-2001	
DT		6,330,696	B1	Zorian et al.	12-11-2001	
DT		6,397,349	B2	Higgins et al.	5-28-2002	

FOREIGN PATENT DOCUMENTS								
Exam. Initial ^a	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (If known)				

Examiner Signature	<i>Davidson</i>	Date Considered	12/6/04
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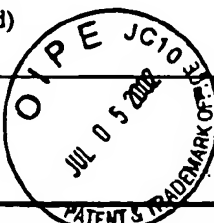
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 4640.P006	Application Number: 10/083,241
	First Named Inventor: Yervant Zorian	
Filing Date: February 25, 2002		



OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
DT		S. SHOUKOURIAN, V. VARDANIAN, Y. ZORIAN, "An Approach for Evaluation of Redundancy Analysis Algorithms", The Proceedings of IEEE Int. Workshop on Memory Technology, Design and Testing, 2001.	
DT		D. K. BHAVSAR, "An Algorithm for Row-Column Self-Repair of RAMs and its Implementation in the Alpha 21264", Proc. ITC'1999, pp. 311-318.	
DT		T. KAWAGOE, J. OHTANI, M. NIRO et al, "A Built-In Self-Repair Analyzer (CRESTA) for embedded DRAMs", Proc. ITC'2000, pp. 567-574.	


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Substitut f r Form 1449/PTO <div style="display: flex; align-items: center; justify-content: space-between;"> <div style="text-align: center;">  </div> <div> INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(use as many sheets as necessary)</small> </div> </div>				Complete if Known	
Application Number		10/083,241			
Filing Date		February 25, 2002			
First Named Inventor:		Yervant Zorian			
Art Unit		2133			
Examiner Name		Unassigned			
Attorney Docket Number		04640.P006			

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number-Kind Code ² (if known)				
DT		US- 6,237,123 B1	05/22/2001	Kim, et al.		
DT		US- 6,205,564 B1	03/20/2001	Kim, et al.		
		US- 6,086,334	07/04/2000	Giles, et al.	<i>previously filed</i>	
DT		US- 6,317,846 B1	11/13/2001	Higgins, et al.		
DT		US- 5,570,374	10/29/1996	Yau, et al.	RECEIVED	
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		Country Code ⁴ Number ⁵ Kind Code ⁶ (if known)				

Examiner Signature	<i>Dawdson</i>	Date Considered	12/6/04
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) JUL 15 2003 Patent & Trademark Office		Application Number	10/083,241
		Filing Date	February 25, 2002
		First Named Inventor:	Yervant Zorian
		Art Unit	2133
		Examiner Name	Unassigned
		Attorney Docket Number	04640.P006
Sheet <u>1</u> of <u>2</u>			
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
DT		Yervant Zorian: "System-Chip Test Strategies" (Tutorial): DAC 1998: 752-757.	
DT		Ilyoung Kim, Yervant Zorian, Goh Komoriya, Hai Pham, Frank P. Higgins, Jim L. Lewandowski: "Built-in Self-Repair for Embedded High Density SRAM." ITC 1998: 1112-1119.	
DT		Yervant Zorian, Erik Jan Marinissen, Sujit Dey: "Testing Embedded-Core Based System Chips." ITC 1998: pages 1-14.	
DT		Yervant Zorian, Erik Jan Marinissen, "System Chip Test: How Will It Impact Your Design?" pages 1-6, DAC, 2000.	
DT		Monica Lobetti Bodoni, Alfredo Benso, Silvia Chiusano, Stefano DiCarlo, Giorgio DiNatale, Paolo Prinetto, "An Effective Distributed BIST Architecture for RAMs," pages 1-6, IEEE European Test Workshop, 2000.	
DT		Chauhin Su, Shih-Ching Hsiao, Hau-Zen Zhau, Chung-Len Lee, "A Computer Aided Engineering System for Memory BIST," pages 1-4, DAC, 2001.	

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